Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E / B. Tech (Full Time) END SEMESTER EXAMINATIONS – NOV/DEC 2024

ELECTRICAL & ELECTRONICS ENGINEERING

EE 7403 Linear Integrated Circuits

(Regulation 2015)

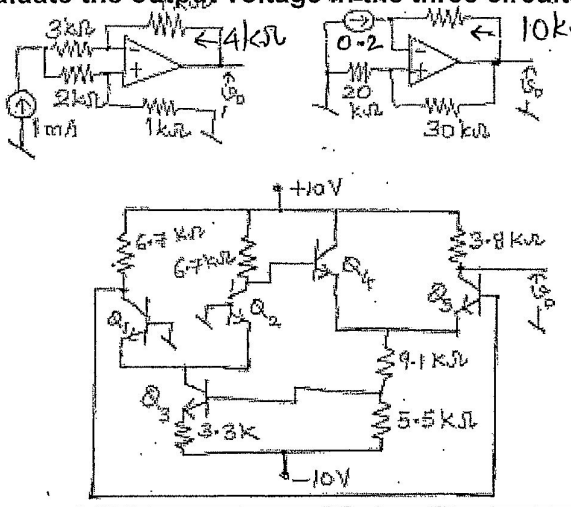
Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART- A (10 x 2 = 20 Marks)

Q.No	Questions	Marks
1.	Given an OPAMP, how would you verify its slew rate specification experimentally?	2
2.	What is an 'Opto-Coupler'? Where is it employed? Give an example for opto-coupler IC?	2
3.	How is a window formed by removal of SiO_2 layer for the purpose of permitting diffusion of impurities?	2
4.	Practically how would you avoid the input offset current of a given OPAMP from giving error in the expected output voltage?	2
5.	What is the purpose for which the pins 5 and 1 of 741 OPAMP are available?	2
6.	Define pull-in time of a PLL?	2
7.	What is the purpose for which the pin 5 of 555 timer IC is available?	2
8.	What are the advantages of ICs over discrete components' based circuits?.	2
9.	What is 'V to I converter'? Give an application for the same.	2
10.	Sketch the circuit diagram of an OPAMP based integrator? Also show that its output voltage is proportional to the integration of input voltage.	2

PART- B (5 x 13 = 65 Marks)

(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks
11.	a) After deriving the relevant expression, design a sine-wave generator based on either Wien bridge Oscillator concept or RC phase-shift oscillator concept for a frequency of 400 Hz. Make suitable assumptions for the design and derivation. State the assumptions made.	13
	OR	
	b) Evaluate the output voltage in the three circuits given alongside:  ← Figure for Q 11 b)	13

12.	a) What are the steps involved in the fabrication of a typical circuit on the silicon wafer? Elaborate.	13
	OR	
	b) What is the significance of 'masking and etching' during the IC fabrication? How is this step repeatedly applied to realize transistor circuits on the tiny wafer? Illustrate with a suitable example circuit.	13
13.	a) How does a 'tri-angular waveform generator' work? Derive an expression for peak-to-peak output voltage and frequency of the tri-angular waveform generated? Explain how would you add wave-shaping circuit to generate sine wave form also apart from the square and tri-angular waveforms?	13
	OR	
	b) Along with block diagram, principle of operation and application examples, discuss in detail ANYTWO of the following topics: i) Linear regulator LM 723 ii) Power amplifier LM 380 iii) Function generator ICL 8038.	13
14.	a) For a transistorized differential amplifier, show that the output voltage can be expressed as : $v_o = -\alpha I_Q \tanh(v_d/2v_T)$, where v_d is the differential input voltage applied and the v_T is voltage equivalent of the ambient temperature. I_Q refers to the current source used in the circuit.	13
	OR	
	b) Distinguish between passive and active filters? Design an OPAMP based 2nd order LPF with a cut-off frequency of 300 Hz. How do you choose the damping factor value for obtaining Butterworth characteristics in filter designed?.	13
15.	a)) i) A 555 timer IC based astable multivibrator is working with T_{on} = 1.5 msec and T_{off} = 1 msec. Now if a diode is added to the circuit (Diode anode is connected to the pin 7 and its cathode point is connected to pin 2), what would be the new frequency of oscillations? Explain. ii) A 555 timer IC based astable multivibrator is working with T_{on} = 1.5 msec and T_{off} = 1 msec. The supply voltage given across pins 8 & 1 is 12 V. Now if pin 5 is supplied with +9 V with respect to ground, what would be the new frequency of oscillations? Explain. (6+7)	13
	OR	
	b). i) Distinguish between 'capture range' and 'tracking range' of a PLL? iii) What is a 'logarithmic amplifier'? How can a multiplier be realized employing log-amplifiers and an anti-log amplifier? iii) How can a XOR gate be used as a digital phase detector? (3+5+5)	13

PART- C (1 x 15 = 15 Marks)

(Q. No 16 is Compulsory)

Q.No	Questions	Marks
16.	.i) Show that in a dual slope type ADC, the final output of the counter is proportional to the input analog voltage. ii) Discuss role of the successive approximation register in the Successive Approximation type ADC. (9 + 6)	15